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REMARKS

Prior to the present amendment and response, claims 1, 3-15, 17-23 and 25 were pending in the present application. By the present amendment and response, independent claims 1 and 14 have been amended to overcome the Examiner's objections and claims 13 and 25 have been canceled. Thus, claims 1, 3-12, 14-15, and 17-23 remain in the present application. Reconsideration and allowance of pending claims 1, 3-12, 14-15, and 17-23 in view of the above amendments and the following remarks are requested.

A. Rejection of Claims 1, 3-15, 17-23, and 25 under 35 USC §103(a)

The Examiner has rejected claims 1, 3-15, 17-23, and 25 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,436,177 to Chiara Zaccherini (hereinafter "Zaccherini") in view of U.S. patent number 5,489,547 to Erdeljac et al. (hereinafter "Erdeljac") and U.S. patent number 6,156,602 to Shao et al. (hereinafter "Shao"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao, singly or in any combination thereof.

The present invention, as defined by amended independent claim 1, includes, among other things, doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the

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second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate. As disclosed in the present application, a first dopant (e.g. an N type dopant) is implanted in a gate region of a polycrystalline layer at a first dose, while a doping barrier prevents the first dopant from being implanted in a resistor region of the polycrystalline layer, where the gate region is situated over a well and the resistor region is situated over a field oxide region, which is not situated over the well. For example, the first dose of the first dopant can be approximately 6.5×10^{15} atoms per square centimeter. As disclosed in the present application, the well and the field oxide region are formed in a substrate.

As disclosed in the present application, after the doping barrier is removed, a second dopant (e.g. a P type dopant) is implanted in the polycrystalline layer at a second dose to determine the resistivity of a resistor subsequently formed in the resistor region of the polycrystalline layer and also implanted in the gate region of the polycrystalline layer. The first dose of the first dopant is significantly higher than the second dose of the second dopant such that the second dose of the second dopant does not affect transistor gate electrical properties. For example, the second dose of the second dopant can be approximately 1.0×10^{15} atoms per square centimeter. As disclosed in the present application, after a high resistivity resistor has been formed in the resistor region of the polycrystalline layer, P+ doped regions are formed by heavily doping uncovered portions

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of the resistor region of the polycrystalline layer with a third dopant (e.g. a P type dopant) having the same conductivity type as the second dopant, and silicide contact regions are formed over the P+ regions. As a result of the above fabrication process, the present invention advantageously achieves a high resistivity resistor having a low fabrication cost and improved electrical connectivity.

In contrast to the present invention as defined by amended independent claim 1, Zaccherini does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate. Zaccherini specifically discloses forming polycrystalline layer 7 over field oxide 5 and channel region 4, where field oxide 5 and channel region 4 are situated on epitaxial layer 3, which is situated on substrate 2. See, for example, column 2, lines 54-55, column 3, lines 1-14, and Figure 3 of Zaccherini. In Zaccherini, a P doped resistor is formed in predetermined area 8 of polycrystalline layer 7 overlying field oxide 5, while a gate terminal is formed over channel region 4. See, for example, column 3, lines 4-6 and 15-23 and Figure 4 of

Zaccherini. In Zaccherini, the P doped resistor and the gate terminal are both situated over epitaxial layer 3.

Thus, Zaccherini fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region and the field oxide region and the well are formed in a substrate, as specified in amended independent claim 1. Also, Zaccherini requires an additional layer (i.e. epitaxial layer 3) to be formed on substrate 2 prior to formation of field oxide 5. Thus, since Zaccherini requires epitaxial layer 3 to be formed on substrate 2 prior to formation polycrystalline layer 7, the structure disclosed in Zaccherini is substantially different than the structure as specified in amended independent claim 1. In particular, the present invention as defined by amended independent claim 1 does not require the additional processing steps of forming and doping an epitaxial layer on a substrate, as required in Zaccherini. Furthermore, Zaccherini provides no motivation for forming a field oxide region and a well directly in a substrate.

Additionally, Zaccherini contemplates implanting an N type dopant at an implant dosage in the range 5×10^{14} to 1×10^{16} ions/cm² in polycrystalline layer 7 directly over channel region 4. See, for example, Zaccherini, column 3, lines 24-36. In Zaccherini, resistors 8 are doped with a P type dopant at an implant dosage of between 1×10^{12} and 1×10^{15} ions/cm². See, for example, Zaccherini, column 3, lines 45-53. Thus, Zaccherini fails to teach, disclose, or suggest doping a layer over a transistor gate region with a first

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dose of a first dopant having a first conductivity type and doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, as specified in amended independent claim 1.

Also, Zaccherini fails to teach, disclose, or suggest doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region, and forming a contact region comprising silicide over the high-doped region, as specified in amended independent claim 1. Moreover, Zaccherini provides no motivation for forming a high-doped region in the layer over the field oxide region. In fact, Zaccherini does not even mention any method of completing formation of the P doped resistor formed in predetermined area 8 of polycrystalline layer 7.

In contrast to the present invention as defined by amended independent claim 1, Erdeljac does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor

gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate. Erdeljac specifically discloses resistors 32 and 34 formed on field oxide region 20, which is formed over P- epitaxial layer 12, and gate 24, which is formed over N well 18 in P- epitaxial layer 12. See, for example, column 1, lines 46-67, column 2, lines 1-6, and Figure 11 of Erdeljac. However, in Erdeljac, P- epitaxial layer 12 is formed on P+ substrate 10 and N well 18 is formed in P- epitaxial layer 12. See, for example, column 1, lines 31-41 and Figures 1 and 2 of Erdeljac. Thus, Erdeljac fails to teach, disclose, or remotely suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region and the field oxide region and the well are formed in a substrate, as specified in amended independent claim 1.

In Erdeljac, a first polysilicon layer is deposited over field oxide region 20 and gate oxide layer 22, heavily doped with an N type dopant, and patterned and etched to form gate 24. See, for example, Erdeljac, column 1, lines 62-65 and column 2, lines 1-10. In Erdeljac, second polysilicon layer 28 is deposited over gate 24 and field oxide region 20, lightly doped with an N type dopant, and patterned and etched to form resistors 32 and 34 on field oxide region 20. See, for example, column 2, lines 15-23, column 5, lines 24-26, and Figures 3 and 11 of Erdeljac. Thus, in Erdeljac, resistors 32 and 34 are formed in second polysilicon layer 28 while gate 24 is formed in a first polysilicon layer. However, Erdeljac fails to teach, disclose, or remotely suggest doping a layer over a transistor gate

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region with a first dose of a first dopant having a first conductivity type and doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, as specified in amended independent claim 1.

Furthermore, Erdeljac fails to teach, disclose, or suggest doping a portion of the layer over the field oxide region with a third dopant so as to form a high-doped region in the layer over the field oxide region and forming a contact region comprising silicide over the high-doped region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, as specified in amended independent claim 1. Thus, Erdeljac fails to cure the basic deficiencies of Zaccherini discussed above.

Also, the resulting structure in Erdeljac, which includes gate 24 and resistors 32 and 34, is substantially different than the structure disclosed in Zaccherini. For example, Zaccherini discloses forming a P doped resistor and a gate terminal in the same polycrystalline layer (i.e. polycrystalline layer 7). In contrast, in Erdeljac, gate 24 is formed in a first polysilicon layer while resistors 32 and 34 are formed in a second polysilicon layer (i.e. second polysilicon layer 28). Thus, for the above reasons, Applicant respectfully submits that there is not sufficient motivation to combine Zaccherini and Erdeljac, as the Examiner suggests.

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In contrast to the present invention as defined by amended independent claim 1, Shao does not teach, disclose, or suggest doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type, doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, where the transistor gate region is situated over a well and the field oxide region is not situated over the well, and where the field oxide region and the well are situated in a substrate. Shao specifically discloses performing N+ implant 18 into poly 2 layer 16 to form the conductivity level of an NMOS poly gate and also to control the value of a load resistor (i.e. load resistor 38), which is also formed in poly 2 layer 16 over field oxide region 12. See, for example, column 5, lines 7-26 and Figures 1 and 5 of Shao.

In Shao, NMOS gate 40 and load resistor 38 are both situated over substrate 10. See, for example, Figure 5 of Shao. However, Shao fails to teach, disclose, or suggest a transistor gate region situated over a well and a field oxide region not situated over the well, where a high resistivity resistor is formed over the field oxide region and the field oxide region and the well are formed in a substrate, as specified in amended independent claim 1. Also, in Shao, an N+ implant is used to dope poly 2 layer 16, which is subsequently patterned and etched to form load resistor 38 and NMOS gate 40. Thus, in contrast to the present invention, load resistor 38 and NMOS gate 40 are not

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independently doped. Furthermore, Shao fails to teach, disclose, or remotely suggest doping a layer over a transistor gate region with a first dose of a first dopant having a first conductivity type and doping the layer over the transistor gate region and a field oxide region with a second dose of a second dopant having a second conductivity type, where the first dose of the first dopant is significantly higher than the second dose of the second dopant such that transistor gate electrical properties are unaffected by the second dose of the second dopant, as specified in amended independent claim 1.

Moreover, Shao fails to teach, disclose, or suggest utilizing a first dopant to dope a transistor gate region, utilizing a second dopant to form a high resistivity resistor in a layer over a field oxide region, and utilizing a third dopant to form a high-doped region in the layer over the field oxide region, where the first dopant has a first conductivity type and the second and third dopants have a second conductivity type, as specified in amended independent claim 1.

Thus, Applicant respectfully submits that the combination of Zaccherini, Erdeljac, and Shao suggest by the Examiner does not and cannot result in the present invention as defined by amended independent claim 1. On page 4 of the Office Action dated December 1, 2004, the Examiner has stated that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zaccherini and Erdeljac with the teachings of Shao. However, the structures and methods of forming the respective structures disclosed in Zaccherini, Erdeljac, and Shao are significantly different from each other. Thus, Applicant respectfully submits that there is

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not sufficient motivation for modifying Zaccherini in view of Erdeljac, and Shao as suggested by the Examiner. In particular, the Examiner has not provided sufficient motivation to modify Zaccherini to include the well as disclosed in Erdeljac and to eliminate an epitaxial layer formed over a substrate, as taught in Zaccherini and Erdeljac. Thus, Applicant respectfully submits that the combined teachings suggested by the Examiner are based on a classic hindsight reconstruction given the benefit of Applicant's disclosure, which is impermissible.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao, singly or in any combination thereof. As such, the present invention, as defined by amended independent claim 1, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 3-12 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Amended independent claim 14 recites similar limitations as amended independent claim 1 discussed above. Thus, for similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by amended independent claim 14, is also not suggested, disclosed, or taught by Zaccherini, Erdeljac, and Shao. As such, the present invention, as defined by amended independent claim 14, is patentably distinguishable over Zaccherini, Erdeljac, and Shao. Thus claims 15 and 17-24

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depending from amended independent claim 14 are, *a fortiori*, also patentably distinguishable over Zaccherini, Erdeljac, and Shao for at least the reasons presented above and also for additional limitations contained in each dependent claim.

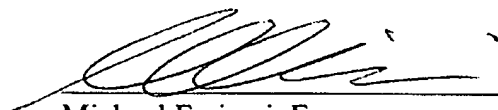
B. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 14, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 3-12, 14-15, and 17-23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 3-12, 14-15, and 17-23 pending in the present application is respectfully requested.

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Respectfully Submitted,
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